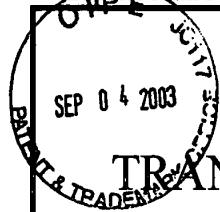


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# TRANSMITTAL FORM

Application Serial Number	09/884,172
Filing Date	June 19, 2001
First Named Inventor	Fitzgerald
Group Art Unit	2812
Examiner Name	Lattin, Christopher W.
Attorney Docket No.	ASC-044
Patent No.	Not applicable
Issue Date	Not applicable

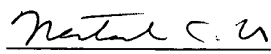
## ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input checked="" type="checkbox"/> Check Attached (\$1,600) <input type="checkbox"/> Copy of Fee Transmittal Form  <input type="checkbox"/> Amendment/Response <input type="checkbox"/> Preliminary  <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Letter to Official Draftsperson including Drawings [Total Sheets ____]  <input type="checkbox"/> Petition for Extension of Time  <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Form PTO-1449 <input type="checkbox"/> Copies of IDS Citations  <input type="checkbox"/> Certified Copy of Priority Document(s)  <input type="checkbox"/> Sequence Listing submission <input type="checkbox"/> Paper Copy/CD <input type="checkbox"/> Computer Readable Copy <input type="checkbox"/> Statement verifying identity of above	<input type="checkbox"/> Copy of Notice to File Missing Parts of Application (PTO-1553)  <input type="checkbox"/> Request For Continued Examination (RCE) Transmittal  <input type="checkbox"/> Copy of Notice of Draftsperson's Patent Drawing Review <input checked="" type="checkbox"/> Formal Drawings (13 sheets)  <input type="checkbox"/> Terminal Disclaimer  <input type="checkbox"/> Executed Declaration and Power of Attorney for Utility or Design Patent Application  <input type="checkbox"/> Small Entity Statement  <input type="checkbox"/> CD(s) for large table or computer program  <input type="checkbox"/> Amendment After Allowance  <input type="checkbox"/> Request for Certificate of Correction <input type="checkbox"/> Certificate of Correction (in duplicate)	<input type="checkbox"/> Notice of Appeal to Board of Patent Appeals and Interferences  <input type="checkbox"/> Appeal Brief (in triplicate)  <input type="checkbox"/> Status Inquiry <input checked="" type="checkbox"/> Return Receipt Postcard <input type="checkbox"/> Certificate of First Class Mailing under 37 C.F.R. 1.8 <input type="checkbox"/> Certificate of Facsimile Transmission under 37 C.F.R. 1.8 <input checked="" type="checkbox"/> Additional Enclosure(s) (please identify below) 1. Transmittal of Issue Fee and Formal Drawings 2. Issue Fee Transmittal (Form PTOL-85B) 3. Comments on Statement of Reasons for Allowance
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## CORRESPONDENCE ADDRESS

Direct all correspondence to: Patent Administrator  
 Testa, Hurwitz & Thibault, LLP  
 High Street Tower  
 125 High Street  
 Boston, MA 02110  
 Tel. No.: (617) 248-7000  
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## SIGNATURE BLOCK

Respectfully submitted,  
  
 Natasha C. Us  
 Attorney for Applicants  
 Testa, Hurwitz & Thibault, LLP  
 High Street Tower  
 125 High Street  
 Boston, MA 02110

Date: September 4, 2003  
 Reg. No. 44,381  
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 Fax No.: (617) 248-7100



*Express Mail Mailing Label No. EV192308481US*

**PATENT**  
Attorney Docket No. ASC-044

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANTS: Fitzgerald et al.  
SERIAL NO.: 09/884,172      GROUP NO.: 2812  
FILING DATE: June 19, 2001      EXAMINER: C. Lattin  
TITLE: METHOD OF FABRICATING CMOS INVERTER AND  
INTEGRATED CIRCUITS UTILIZING STRAINED SILICON  
SURFACE CHANNEL MOSFETS

Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE**


Sir:

In response to the Examiner's statement of reasons for allowance included in the Notice of Allowability mailed from the U.S. Patent Office on June 6, 2003, Applicants note that the prior art fails to adequately anticipate or obviate a method of providing a heterostructure including a Si substrate, a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer on the substrate, and a strained surface layer on the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer, with a planarized surface between the strained surface layer and the substrate having a roughness of less than 1 nm, and integrating a p- and an n-MOSFET in the heterostructure with channels of the p- and n-MOSFETS formed in the strained surface layer.

Respectfully submitted,

Date: September 4, 2003  
Reg. No. 44,381

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\_\_\_\_\_  
Natasha C. Us  
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125 High Street  
Boston, Massachusetts 02110



**PATENT**

Atty Docket No. ASC-044 (366/72)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANTS: Fitzgerald *et al.*

SERIAL NO.: 09/884,172      GROUP NO.: 2812

FILED: June 19, 2001      EXAMINER: Lattin, Christopher W.

TITLE: METHOD OF FABRICATING CMOS INVERTER AND  
INTEGRATED CIRCUITS UTILIZING STRAINED SILICON  
SURFACE CHANNEL MOSFETS

Mail Stop ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313

**TRANSMITTAL OF ISSUE FEE AND FORMAL DRAWINGS**

In response to the NOTICE OF ALLOWANCE AND ISSUE FEE DUE mailed on  
June 6, 2003, attached please find:

- (a) Issue Fee Transmittal (Form PTOL-85B); and
- (b) a check in the amount of \$1,600.00 for payment of Issue Fee and Publication Fee..

In response to the NOTICE OF ALLOWABILITY mailed on June 6, 2003, attached  
please find the formal drawings for this application (Number of Sheets - 13).

Applicants submit that no new matter is added and respectfully request that the proposed  
formal drawings be considered and entered.

Respectfully submitted,

Date: September 4, 2003

A handwritten signature in cursive script, appearing to read "Natasha C. Us".

Natasha C. Us,  
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